

Return To Potentiometers With Reliability: Digital Potentiometers

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Resistor potentiometers can be found in electronic circuits across a wide spectrum of applications. Typically they function in configurations where they are used to execute offset or adjust gain. Until recently the mechanical potentiometer has been the only one of choice, having a wide variety of values available and tight specifications; such as nominal resistance and temperature. But in many applications the over-riding factors against using the mechanical potentiometer are related to environmental, reliability, and repeatability issues. These short-comings have contributed to the adoption of alternative circuit solutions.

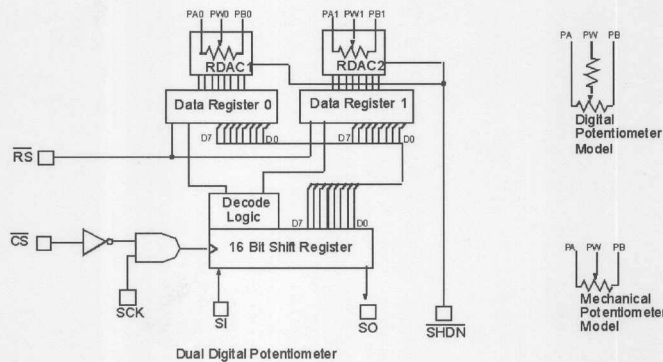
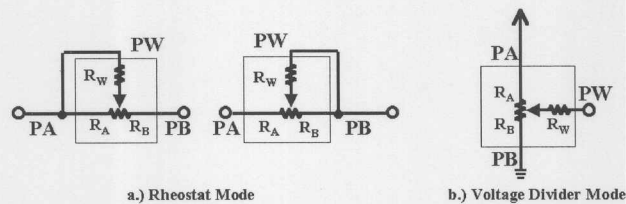


Figure 1. The operation of the digital potentiometer as compared to the mechanical potentiometer is functionally the same. The adjustment of the digital potentiometer is done with a serial code to the device.

The digital potentiometer (Fig. 1) brings the designer back to the potentiometer element by providing a reliable alternative, offering a solution with superior environmental tolerance to shock and improved mechanical reliability because of the absence of the mechanical wiper. In addition to these improvements, the digital potentiometer has programmability which is a significant advantage as microcontrollers and microprocessors continue to dominate the total electronic solution. The programmability also allows the user to repeatedly and reliably return to the same wiper position.

Any potentiometer can be configured in one of two modes -- rheostat and voltage. In a circuit where the potentiometer is used in the rheostat mode, the wiper (terminal PW), is shorted to either the PA or PB terminal of the device (Fig. 2a.) When a digital potentiometer is used in the voltage divider mode (Fig. 2b) all three terminals are connected to differing nodes in the circuit. In both of these configurations, the digital potentiometer will have a nominal resistance and temperature coefficient error that may affect the overall application unless design precautions are taken. The circuit ideas presented in this article use the necessary design techniques to mitigate these errors, consequently optimizing the performance of the digital potentiometer, making it a very strong contender for the mechanical potentiometer.



Device	Nominal R_{AB} Resistance (typ)	R_{AB} Change with Temp (typ)	Nominal Resistance Match (typ)	R_A, R_B Relative Accuracy INL (typ)	Tempco Variance Between R_A and R_B (typ)	Code to Code Variance DNL (typ)
MCP41010 (single)	$10k\Omega \pm 20\%$	800ppm / °C	----	$\pm 0.1\%$	1 ppm / °C	$\pm 0.1\%$
MCP42010 (dual)	$10k\Omega \pm 20\%$	800ppm / °C	0.2%	$\pm 0.1\%$	1 ppm / °C	$\pm 0.1\%$
MCP41050 (single)	$50k\Omega \pm 30\%$	800ppm / °C	----	$\pm 0.1\%$	1 ppm / °C	$\pm 0.1\%$
MCP42050 (dual)	$50k\Omega \pm 30\%$	800ppm / °C	0.2%	$\pm 0.1\%$	1 ppm / °C	$\pm 0.1\%$
MCP41100 (single)	$100k\Omega \pm 30\%$	800ppm / °C	----	$\pm 0.1\%$	1 ppm / °C	$\pm 0.1\%$
MCP42100 (dual)	$100k\Omega \pm 30\%$	800ppm / °C	0.2%	$\pm 0.1\%$	1 ppm / °C	$\pm 0.1\%$

Figure 2. The resistive elements of the digital potentiometer can be configured the Rheostat mode (a) or the Voltage Divider mode (b). Each mode has its own set of performance specifications.

Digital Potentiometer Circuits Configured In The Rheostat Mode

In the rheostat mode either terminal PA or PB are connected to the wiper terminal (Fig. 2a) and the output resistance is digitally-adjusted from the maximum nominal value, minus one LSB, down to zero ohms. The nominal resistance of the element in the rheostat mode is calculated with the following formulas:

$$R_{BW} = R_{AB} (D_n)/2^n + R_W$$

$$R_{AW} = R_{AB} (2^n - D_n)/2^n + R_W,$$

Where,

R_{AW} is the resistance across the A element of the digital potentiometer plus the wiper resistance,

R_{AB} is the nominal resistance across the entire potentiometer, from pin A to pin B,

R_{BW} is the resistance across the B element of the digital potentiometer plus the wiper resistance.

n is the number of digital potentiometer bits (8 for the MCP4xxxx family of potentiometers from Microchip,)

D_n is the digital code in decimal form that is used to program the digital potentiometer (0 to $2^8 - 1$ or 255 for 8-bit pots.)

R_W is the parasitic resistance through the wiper.

As summarized in the table (Fig. 2) the nominal resistance of the digital potentiometer varies depending on the device selected. Additionally, part-to-part variation of the nominal resistance is specified to be within a given percentage. For example, the nominal resistance of the MCP4x0010 is $10k\Omega \pm 20\%$. The resistance variation of these digital potentiometers is primarily dependent on the process variation of the sheet-rho of a diffused p-silicon layer and the on-resistance of the internal switches.

The temperature variance of the digital potentiometer element is also shown (Fig. 2); for instance, the variance of the MCP41010 ($10k\Omega$) digital potentiometer is 800ppm/°C (typical). With this specification the expected change of the total resistance of the MCP41010 is from $10k\Omega$ at 25°C to $10.488k\Omega$ at 85°C or a delta of 488 Ω .

The level of nominal resistive matching that is shown (Fig. 2) can be acceptable for some applications. However, if a degree of precision is desired, the dual potentiometer can be used to an advantage in the rheostat mode. With the dual digital potentiometer, the nominal resistances between the two potentiometers are ratio-matched to a very small percentage (per Fig. 2.) For instance, the matching of the two resistive potentiometer elements in the MCP42010 (dual, 10 k Ω) is guaranteed to be less than $\pm 0.2\%$ (typ.) This close relationship between the two resistor arrays can be used to a distinct advantage.

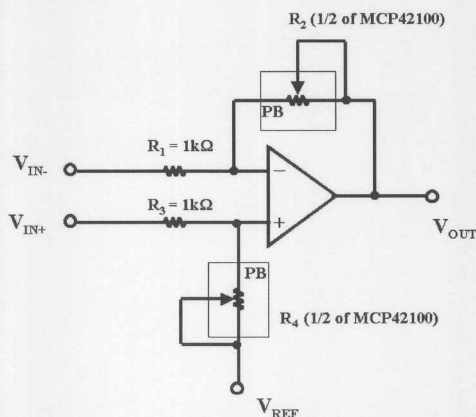


Figure 3. The digital potentiometers in this differential amplifier can be programmed to change the gain of the circuit as well as enhance the common-mode rejection. The common-mode rejection of this circuit is fairly immune to temperature changes.

In one circuit (Fig. 3) that takes advantage of the relationship between the two potentiometers in the dual, MCP42100, the arrangement of the resistors around an operational amplifier is called the difference amplifier or op amp subtractor. The dc transfer function of this circuit is equal to,

$$V_{OUT} = V_1 R_4 (R_1 + R_2) / ((R_3 + R_4) R_1) - V_2 (R_2 / R_1) + V_{REF} R_3 (R_1 + R_2) / ((R_3 + R_4) R_1)$$

If R_1/R_2 is equal to R_3/R_4 , the system gain of this circuit equals,

$$V_{OUT} = (V_1 - V_2) (R_2 / R_1) + V_{REF}$$

The fact that R_1/R_2 is equal to R_3/R_4 simplifies the mathematics in this system considerably. Since the gain of both input signals are the same, the common-mode voltage (CMV) of the two signals is conveniently subtracted from the output results.

Ideally, CMV changes are rejected by this circuit. The calculated common-mode rejection (CMR) error that is attributed to resistor mismatches in this circuit is equal to,

$$CMR = 100 * (1 + R_1/R_2) / (\% \text{ of mismatch error})$$

where (% of mismatch error) is the mismatch in the equation $R_1/R_2 = R_3/R_4$

An example of the impact of this error is demonstrated with a 12-bit, 5-V system, where the gain of the circuit is 100 V/V, the common-mode voltage ranges 0 to 5 V and the matching error is $\pm 0.2\%$. Using the formula, above, the contributed error of a common-

mode excursion from 0 to 5 V is equal to 0.2 mV. This voltage is six times less than 1 LSB in this 12-bit system. Adjustable gain is easily implemented by making the discrete resistors equal ($R_1=R_3$) and changing both potentiometers together as desired.

In a single-supply environment a voltage reference is used to center the output signal between ground and the power supply, represented in this circuit as " V_{REF} ". The V_{REF} circuit function can be implemented with a precision voltage reference or with an adjustable voltage reference circuit that uses a digital potentiometer (shown, later, in Figs. 5, 6 and 7.) The adjustable voltage reference designs offer the flexibility of removing offset system errors.

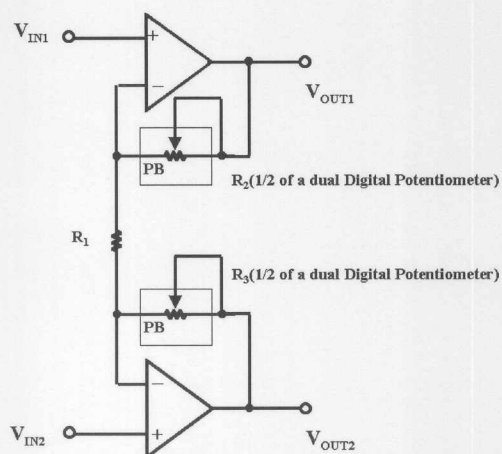


Figure 4. This differential in and differential out circuit uses two digital potentiometers in the Rheostat mode. When the two digital potentiometers are set to be equal, the gains on the two input signals are equal.

An alternative to the circuit of Fig. 3 is that of Fig. 4 where the differential inputs are high impedance and the output is differential. There are three resistors used in this circuit, two of which are 1/2 of a dual potentiometer.

If $R_2 = R_3$, the transfer function of this circuit is,

$$(V_{OUT1} V_{OUT2}) = (V_{IN1} V_{IN2})(1 + 2R_2/R_1)$$

This flexible gain circuit uses the matching of nominal resistance and thermal shifts of the dual potentiometer to an advantage.

Digital Potentiometer Circuits Configured In The Voltage Divider Mode

In the voltage divider mode (Fig. 2) all three terminals to the potentiometer are connected to separate nodes in the circuit. In this mode, the total resistance of the device is separated into two resistors. The first being the resistance at terminal PB and the second is at terminal PA. The relationship between these two resistors is equal to,

$$R_B = R_{AB} (D_n)/2^n$$

$$R_A = R_{AB} (2^n - D_n)/2^n$$

Where, R_B is equal to the resistance of the element B and, R_A is equal to the resistance of the element A.

A third resistance can be found from each element (A and B) through the wiper terminal, PW, called the wiper resistance or R_W . If the wiper of the digital potentiometer is followed by a high impedance node, this resistance can be ignored.

The absolute value of elements A and B will still vary between $\pm 20\%$ and $\pm 30\%$ (depending on the device used) however, as shown in the table (Fig. 2), the ratio between the two elements will be much lower. In the case of the MCP4x010, the maximum mismatch error between R_B and R_A is $\pm 0.1\%$ (DNL specification.)

Since the resistive elements of R_B and R_A are manufactured with the same material on the same chip, the ratio of the thermal changes with temperature is considerably better as compared to the single resistive element in the rheostat mode. The temperature performance between these two elements (A and B) is also lower than the absolute temperature behavior, at a typical $1\text{ppm}/^\circ\text{C}$.

The digital potentiometer can be used very effectively in a variety of circuits when it is configured in the voltage divider mode. All of the following circuits take advantage of the resistive ratio matching of the two resistive elements (R_B and R_A .)

Voltage Reference Circuits

One form of offset-voltage adjustment can be implemented with a voltage reference. This type of adjustment usually compensates for all of the system offset errors in the signal path. A digital potentiometer (Fig. 5) is used to design an adjustable voltage reference. In circuit (a) the potentiometer is placed between the positive power supply and ground. The output voltage of the adjustable reference is equal to,

$$V_{\text{REF}} = V_{\text{DD}} R_{\text{POT-B}} / R_{\text{POT-AB}}$$

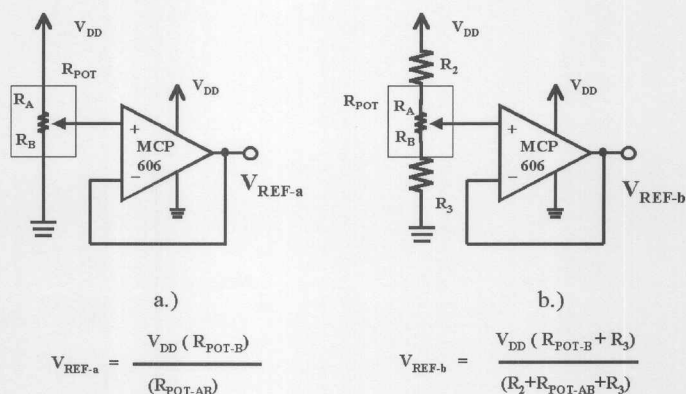


Figure 5. A digitally adjustable reference can be designed using the power supply across the digital potentiometer (a). Higher accuracy can be achieved by using additional resistors (b) in series with the digital potentiometer.

The resolution of this reference circuit is dependent on the number of programmable bits of the digital potentiometer and the value of V_{DD} . When using any of the 8-bit digital potentiometers and a 5-V supply, the nominal LSB size would be 19.53 mV. In this

circuit the operational amplifier acts to isolate or buffer the digital potentiometer resistance from the following circuitry.

The absolute accuracy and over temperature performance of the voltage presented to the input of the amplifier is dependent on the matching of the digital potentiometer resistive elements as well as the stability of the power supply. As an example of the effects of the digital potentiometer errors, the MCP4x010 (10k Ω) would perform with an absolute accuracy less than $\pm 0.1\%$ (± 0.25 LSB) or ± 4.883 mV at 25°C. Over temperature the output voltage would typically vary 1% due to resistance matching. This translates into a typical variance over temperature (-40°C to +85°C) of 0.195 mV or ± 97.7 μ V. Adding this to the error at room temperature, the total possible error becomes ± 4.93 mV. In this example it is assumed that the power supply is a stable 5V.

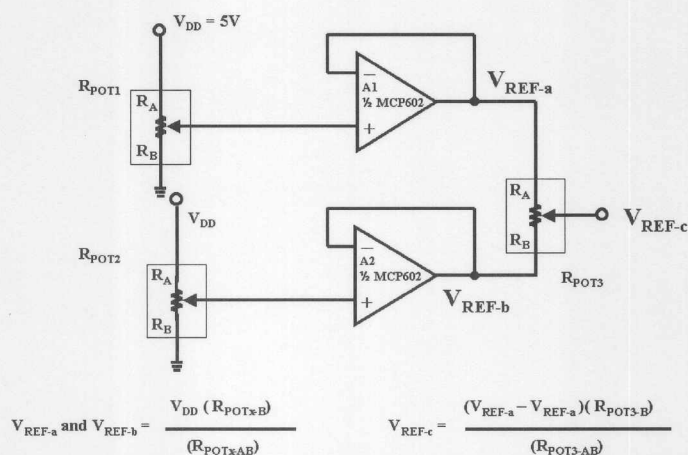


Figure 6. Three digital potentiometers in combination with a dual amplifier can be configured for a wide dynamic range, adjustable voltage reference that has an ideal LSB size of $V_{DD}/2^{2n}$, where n is the number of digital potentiometer bits.

If a smaller LSB size is required for an adjustable voltage reference that has the full dynamic range of the power supply voltage, a circuit (Fig. 6) can be used where the wiper voltage of R_{POT1} is buffered with A1 (a single supply CMOS amplifier) and R_{POT2} is buffered with A2. The dynamic range of the output of A1/A2 is equal to approximately (GND+50 mV) to (V_{DD} 1.2 V.) The positive output swing range is primarily restricted by the amplifiers' maximum input common-mode voltage. The theoretical LSB size of the voltages at V_{REF-a} and V_{REF-b} are equal to $V_{DD}/2^n$ or 19.53 mV. The voltage difference of V_{REF-a} and V_{REF-b} is impressed across R_{POT3} . The difference of these voltages is then divided again by the third digital potentiometer to have an ideal LSB size equal to,

$$V_{REF-C} = (V_{DD}/2^n)/2^n = V_{DD}/2^{2n}$$

The configuration in Fig. 6 provides a theoretical output resolution of 16-bits. When V_{DD} is equal to 5 V, the theoretical LSB size is 76.29 μ V. The value of the output of this precision adjustable reference is compromised by the absolute matching resistance and temperature coefficient of the digital potentiometers.

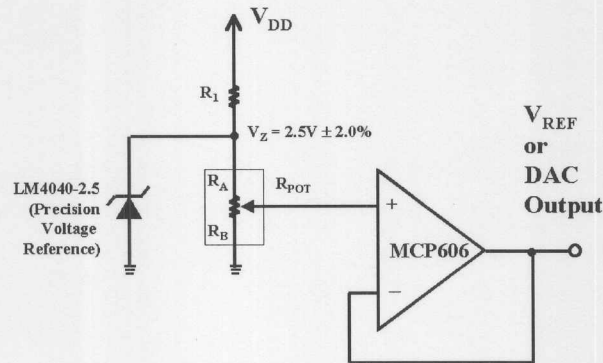


Figure 7. A precision adjustable reference can be configured using a precision reference that is not adjustable along with a digital potentiometer. The value of R_1 is set so that the current through the LM4040 does not go below its minimum operating current.

Another technique that can be used to design a precision adjustable voltage reference is shown in Fig. 7. In this circuit the variability of the power supply is stabilized with a precision voltage reference. Since the digital potentiometer is configured in the voltage divider mode the errors at the output of the amplifier are similar to those errors in Fig. 5, the only difference being that the power supply is replaced with a precision reference. This configuration is often used when the digital potentiometer is used as a DAC.

Offset Adjustment Circuits

Offset adjustment can be implemented in the analog circuit by injecting a voltage into the signal path with a simple voltage divider or a complete adjustable voltage reference.

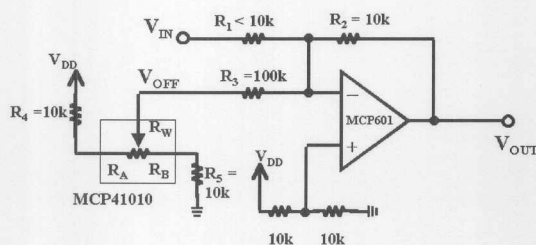


Figure 8. A high resolution offset adjust circuitry is implemented in this standard inverting amplifier configuration with the addition of a digital potentiometer, R_3 , R_4 and R_5 .

In Figs. 8 and 9, a digital potentiometer is used to change the offset errors of a simple amplifier circuit. In this circuit, the amplifier is configured in an inverting configuration. The transfer function for the input signal, V_{IN} is equal to,

$$V_{OUT} = V_{IN}(R_2/R_1) + V_{DD}/2$$

An offset voltage is injected with the same voltage divider that was used in the circuit in Fig. 5b. The transfer function of the offset voltage, V_{OFF} , is,

$$V_{OUT} = V_{OFF} (R_2/R_3)$$

With the resistor values shown the gain on the V_{IN} is 10 V/V and the gain of V_{OFF} is 0.1 V/V. With $V_{DD} = 5$ V, the LSB size of the offset adjust circuitry is 651 μ V. With this configuration the nominal errors and over-temperature errors that are generated by the digital potentiometer are 10x smaller than the errors in Fig. 5b.

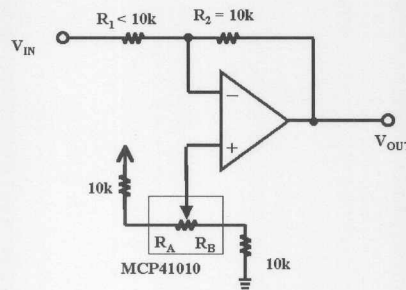


Figure 9. A lower resolution offset adjust circuit using a digital potentiometer can be used to adjust large system offsets.

Another method of implementing an analog offset adjustment with a digital potentiometer is shown in Fig. 9. In this circuit the gain of the signal is equal to,

$$V_{OUT} = V_{IN}(R_2/R_1)$$

And the gain of the offset adjust circuitry is equal to,

$$V_{OUT} = V_{DD}R_{POT-B}(1+R_2/R_1)/(R_{POT-AB}+R_2+R_3)$$

The offset adjustment circuit that is used in Figs. 8 and 9 has the same topology as that of Fig. 5b. So, the errors due to this configuration are consistent with previous discussions.

Gain-Adjust Amplifier Circuits

Circuit gain errors can compromise the analog dynamic range of a circuit. These types of errors can be easily digitally calibrated out of the system with the microcontroller, however, the analog dynamic range is never fully used. Consequently analog gain adjustments are done where the full dynamic analog range is needed. An example of an amplifier circuit that has an adjustable positive (non-inverted) gain is shown in Fig. 10. In this circuit, the transfer function is,

$$V_{OUT} = V_{IN} (1 + R_3/R_2)(R_{POT1-B}/(R_{POT1-AB}))$$

The adjustable gain is implemented with the digital potentiometer, R_{POT} . Digital potentiometers of have higher values are best suited for this circuit as they minimize the error that is contributed by the source resistance of V_{IN} .

The maximum gain of this circuit equals,

$$\text{Gain (max)} = (1 + R_3/R_2) (2^n - 1)/2^n$$

Using the values of resistors in Fig. 10,

$$\text{Gain (max)} = (1 + 100 \text{ k}\Omega/1 \text{ k}\Omega)(2^8 - 1)/2^8 = 101.996 \text{ V/V}$$

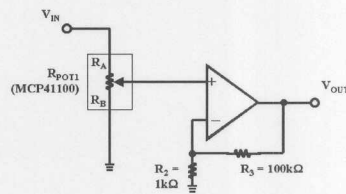


Figure 10. An amplifier circuit designed with an adjustable non-inverting gain.

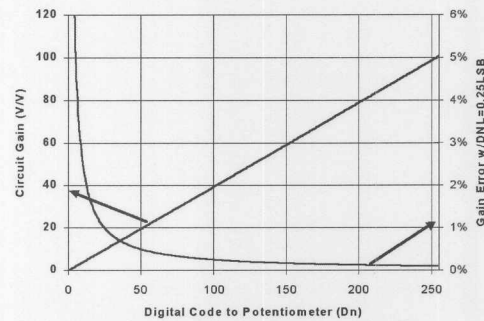


Figure 11. For the circuit in Figure 10, the gain vs digital code is linear. The maximum possible gain error is logarithmic, decreasing with higher digital potentiometer codes.

At room temperature, the digital potentiometer's DNL error affects the circuit gain accuracy with gains that are lower 10% of the range (assuming $DNL(\text{max}) = \pm 0.4\%$ or $\pm 0.25 \text{ LSB}$). This relationship is shown graphically in Fig. 11.

In terms of temperature effects on the digital potentiometer in this configuration, the changes of R_A and R_B over temperature track at a rate of $800 \text{ ppm}/^\circ\text{C}$ (typ.) Since these elements are configured as a mathematical ratio this error is cancelled. The variance between the two elements over temperature is 1% (typ.) This variance is directly translated into gain error over temperature.

Another amplifier circuit that uses a digital potentiometer is shown in Fig. 12 where the amplifier executes an inverting adjustable gain function with a circuit transfer function,

$$V_{OUT} = V_{IN}(R_{POT2-A}/R_{4-B}) + V_{REF}(R_{POT2-A}/R_{POT2-B} + 1)$$

With this circuit, gain function vs. digital potentiometer code is non-linear as shown in Fig. 13.

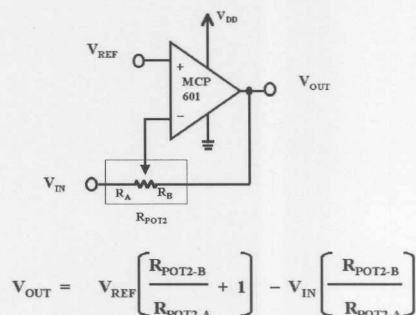


Figure 12. This amplifier circuit uses a digital potentiometer to implement an adjustable inverting gain.

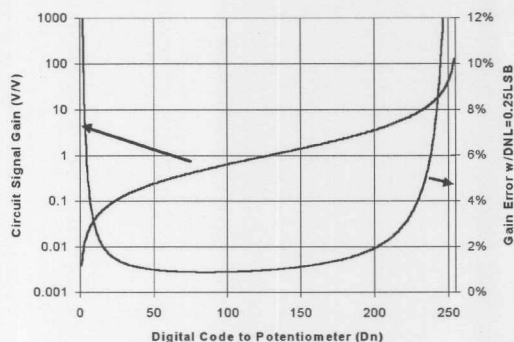


Figure 13. The transfer function of V_{OUT} to V_{IN} of the circuit shown in Figure 12 has a non-linear response over the code span of the digital potentiometer. The circuit that gains the input signal below digital potentiometer codes of 128 and attenuates the signal with codes above 128.

The nominal accuracy of this gain cell is minimized because the two sides of the digital potentiometer are ratioed in the circuit transfer function. Any gain error at room temperature is due to the DNL error of the digital potentiometer. The maximum effects of this error is shown graphically in Fig. 13.

In terms of temperature effects on the digital potentiometer in this configuration, R_A and R_B are configured as a mathematical ratio in the transfer function. This cancels the change in the 800 ppm/°C (typ) resistive element. The variance between the two elements over temperature is 1% (typ) which will be directly translated as gain error over temperature.

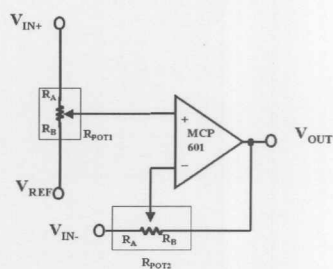


Figure 14. A difference amplifier that has stable resistor matching and temperature coefficients.

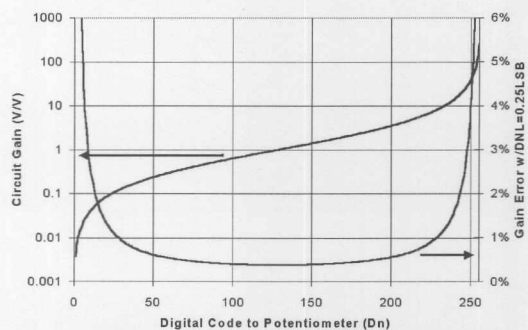


Figure 15. The gain of circuit in Figure 14 is greater than one with digital code settings larger than 128 and between zero and one for digital code settings less than 128. The gain error, due to typical DNL errors, is less than 1% between 28 and 229.

The circuits in Figs. 10 and Figure 12 can be combined to build an adjustable-gain difference amplifier much like the circuit shown in Fig. 3 with the configuration shown in Fig. 14.

If the digital code settings for R_{POT1} and R_{POT2} are equal, the transfer function for this circuit is,

$$V_{OUT} = (V_1 - V_2)(R_{POTx-B}/R_{POTx-A}) + V_{REF}$$

The gain of this circuit ($V_{OUT}/(V_1 - V_2)$) versus the digital potentiometer code is shown graphically in Fig. 15.

The temperature performance of this circuit is significantly improved over the circuit in Fig. 3 because all of the resistors in this circuit are elements of the digital potentiometers. Once again, the common-mode rejection (CMR) error that is attributed to resistor mismatches in this circuit equals,

$$CMR = 100 * (1 + R_1/R_2) / (\% \text{ of mismatch error})$$

Where, (% of mismatch error) is the mismatch in the equation $R_1/R_2 = R_3/R_4$

Conclusion

The digital potentiometer has entered the market with clear advantages over the mechanical potentiometer. Its programmability allows changes in offset, gain and voltage references circuits reliably as well as on the fly. Digital potentiometers have been criticized because of their absolute variation from part-to-part and tempco. With clever designs, these apparent short comings can easily be overcome.

References:

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- "The Potentiometer Handbook: Users' Guide to Cost-effective Applications," Todd, Carl David, McGraw-Hill, 1975